Amendments to Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A test method comprising:

[[a)]] providing first, second and third test structures on a wafer~~, each having respective~~ with first, second and third test structure parameters comprising resistive portions from which test measurement values of resistances are measured, wherein the resistive portions comprise effective lengths and effective widths;

[[b)]] obtaining test measurement values from the test structures ~~each of the first, second and third test structures at least one test measurement value, the test measurement values varying based on the first, second and third test structure parameters~~;

[[c)]] calculating a goodness of fit value for a fitted curve between the effective lengths divided by the test measurement values and the effective widths of the resistive portions

~~(1) said test measurement values, and~~

~~(2) values of the first, second and third test structure parameters, wherein the goodness of fit value comprises an evaluation of difference between predicted values and test measurement values obtained~~; and

[[d)]] using said goodness of fit value to monitor processes used to form a device.

2. (currently amended) The method of claim 1 ~~wherein step d)~~ further comprises ~~includes~~ using control limits on the goodness of fit value and using said goodness of fit value to[[: (1)]] control the processes used to form the device or [[(2)]] to screen the device.

3. (currently amended) The method of claim 1 ~~wherein step d)~~ further comprises:

~~includes~~ using control limits on the goodness of fit value[[; said]], wherein the control limits are established based on a history of goodness of fit values or on device requirements; and

using said goodness of fit value to[[: (1)]] control the processes used to form the device or [[(2)]] to screen the device.

4. (previously presented) The method of claim 1 wherein the goodness of fit value is a correlation coefficient or a standard error measurement.

5. (currently amended) The method of claim 1 wherein the fitted curve is a[[t]] least squares fitted straight line.

6. (currently amended) The method of claim 1 ~~wherein the test measurement values are resistance or capacitance measurements values; and step d)~~ further comprises using [[said]] the goodness of fit value to[[: (1)]] control the processes used to form the device or [[(2)]] to screen the device.

7. (previously presented) A test method comprising:

a) providing a device structure that has at least a first test structure, a second test structure and a third test structure incorporating resistive portions from which resistance is measured;

(1) said resistive portions having an effective length (Lx) and an effective width (Wx),

(2) said first, second and third test structures have resistive portions with different effective widths (W1 W2, … Wi);

(3) said resistive portions of said first, second and third test structures have effective lengths (L1, L2, …Li);

b) measuring the resistance (R) of the test structures;

c) calculating a goodness of fit value for a fitted curve between:

(1) said effective lengths divided by the measured resistances (L1/R1, L2/R2, …L1/Ri); and

(2) the effective widths (W1, W2, .. Wi) of the resistive portions of the test structures;

d) using said goodness of fit value to: (1) control processes used to form the device structure or (2) screen the device structure.

8. (original) The method of claim 7 wherein said fitted curve is a fitted straight line fitted using a least squares method.

9. (original) The method of claim 7 wherein said test structures are formed in and/or over a wafer.

10. (original) The method of claim 7 wherein said test structures are comprised of a doped region in a wafer.

11. (canceled)

12. (original) The method of claim 7 wherein said test structures are comprised of a conductive material and an interconnect layer in a semiconductor device is comprised of said conductive material.

13. (original) The method of claim 7 wherein said test structures are comprised of metal from a metal layer that is used to form metal lines in a semiconductor devices.

14. (original) The method of claim 7 wherein said test structures are comprised of a material selected from the group consisting of silicon, amorphous silicon, polysilicon, polycide, silicide, metal, copper, aluminum, and alloys and combinations thereof.

15. (original) The method of claim 7 wherein said goodness of fit value is a correlation coefficient, coefficient of determination or standard error measurement test.

16. (previously presented) The method of claim 7 wherein said resistive portions have said effective lengths being substantially greater than said effective widths, and said effective widths being selected to be substantially greater than an expected critical dimension loss for said processes.

17. (previously presented) The method of claim 7 wherein the measuring the resistance (R) of the test structures comprises measuring the resistance at different temperatures; and further includes: calculating the goodness of fit value for a straight line for the between:

(1) the effective lengths divided by the measured resistances (L1/R1, L2/R2, ..Li/Ri).; the effective lengths of the test structures are equal(L1 = L2 = ..Li); and

(2) the effective widths (W1, W2, ..Wi) of the test structures; and

(3) the temperature.

18. (previously presented) The method of claim 7 wherein said device structure is a wafer; said wafer has at least three test structures;

the goodness of fit value is calculated on measurements made on the test sites on said wafer.

19. (previously presented) The method of claim 7 wherein said device structure is a printed circuit board, a ceramic substrate or a chip scale package.

20. (previously presented) The method of claim 7 wherein structures are formed adjacent to said resistive portion to measure effects of micro loading or chemical-mechanical polishing.

21. (previously presented) A method for estimating defect levels by measurements related to resistance of an interconnect layer in a process for manufacturing an integrated circuit, said method comprising the steps of:

a) fabricating on a wafer, using processes, at least a first test structure, a second test structure and a third test structure incorporating a resistive portion from which a resistance is measured;

b) said resistive portion having an effective length and an effective width, said effective length being substantially greater than said effective width, and said effective width being selected to be substantially greater than an expected critical dimension loss for said processes;

c) measuring said resistance of the test structures; and

d) deriving the sheet resistances from the resistance measurements;

e) calculating a goodness of fit value between the one divided by the sheet resistances (1/Rs) and a second parameter;

f) using said goodness of fit value to: (1) control the processes used to form the test structures or (2) screen the test structures.

22. (original) The method of claim 21 where said second parameter is the effective width of the test structures or the temperature.

23. (currently amended) A test method comprising:

[[a)]] providing a device structure that has at least [[a]] first, second and third test structures, ~~a second test structure and a third test structure on the substrate~~ the test structures comprise resistive portions having effective lengths and widths from which a test parameter of resistance is measured;

[[b)]] measuring test parameter values on the test structures;

[[c)]] calculating a goodness of fit value for a fitted curve between[[:]] the effective lengths divided by the test parameter values and the effective widths of the resistive portion

~~(1) the test parameter values and~~

~~(2) a dimensional measurement of the test structures, wherein the goodness of fit value is based on an evaluation of difference between predicted values and test parameter values measured~~;

d) using said goodness of fit value to[[: (1)]] control [[the]] processes used to form the device structure or [[(2)]] to screen the device structure.

24. (cancelled)

25. (currently amended) A test method comprising:

[[a)]] providing a device structure on a wafer that has a plurality of test structures with respective test structure parameters;

[[b)]] measuring a first test measurement, a second test measurement and a third test measurement on at least ~~one of the~~ a first test structure, wherein the first test structure is a

resistance test structure that has a effective length (L) and effective Width (W), the first test measurement is a resistance test measurement;

[[c)]] calculating a goodness of fit value for a fitted curve between at least,

[[(1)]] the first test measurement performed under a first test condition,

[[(2)]] the second test measurement performed under a second test condition, and

[[(3)]] the third test measurement performed under a third test condition,

wherein the test conditions have different temperatures,

wherein the goodness of fit value is for a straight line fitted to the effective length (L) divided by the resistance (R) vs. the effective width (W) ~~is based on an evaluation of difference between predicted values and test measurement obtained~~; and

[[d)]] using [[said]] the goodness of fit value to [[(1)]] control processes used to form the device structure or [[(2)]] to screen the device structure.

26. (previously presented) The method of claim 25 wherein: said first test condition, said second test condition and said third test condition are different temperatures.

27-29. (cancelled)

30. (previously presented) The method of claim 1 wherein the test measurement values are obtained on two or more test sites on the device.

31-32. (cancelled)

33. (previously presented) The method of claim 1 wherein the first, second and third test structure parameter comprises an area of a capacitive portion of the respective first, second and third test structure.

34. (cancelled)

35. (currently amended) A method of forming a device comprising:

providing test structures on a wafer, the test structures having respective test structure parameters comprising resistive portions from which test measurement values of resistances are measured, wherein the resistive portions comprise effective lengths and effective widths;

obtaining test measurement values which are based on the test structure parameters;

determining a goodness of fit value based on the effective lengths divided by the test parameter values and the effective widths of the resistive portion ~~difference between predicted values fitting a curve from test measurement values obtained~~; and

screening wafers on which devices are formed based on a scrap limit established from the goodness of fit value.

36. (new) The method of claim 35 wherein test measurements are performed under test conditions.

37. (new) The method of claim 35 wherein test measurements are performed under respective test conditions.

38. (new) The method of claim 35 wherein the test conditions comprise different temperatures.

39. (new) The method of claim 38 wherein the goodness of fit value is for a straight line fitted to the effective length divided by the resistance verses the effective width.

40. (new) The method of claim 35 wherein the goodness of fit value is for a straight line fitted to the effective length divided by the resistance verses the effective width.